

REMARKS

Claims 1-10, 19, and 20 are all the claims presently pending in the application. Claims 11-18 are withdrawn but subject to rejoinder. Claims 5 and 12 have been amended to more particularly define the invention and address the Examiner's objection.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1, 4-6, and 19 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

Claims 1-6, 8-10, and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,869,844 to Liu et al. Claims 7 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu, further in view of US Patent 6,815,771 to Kimura.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to an electronic chip including a first circuit design module having a first grid and a second circuit design module having a second grid. The first grid and the second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in the fabrication.

As explained beginning at paragraph [0039], the conventional practice in SOI circuit design and fabrication is that the various circuit design modules are interconnected in the final metallization step (e.g., M5).

The claimed invention, on the other hand, teaches that the charging due to plasma processing is not distributed uniformly over the two-dimensional surface of the chip. Therefore, the plasma processing can cause differential voltages across the chip, including, particularly, differential voltages between the grids of the various design modules on the chip. To preclude this differential voltage condition, the present invention teaches that the design modules should

be interconnected prior to the final metallization that is taught by conventional wisdom.

II. THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claims 1, 4-6, and 19 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. Applicants respectfully disagree, as described below.

Relative to claims 1 and 19, the Examiner alleges that the final claim limitation renders the claim indefinite because, according to the Examiner, it is confusing because the figures show that the first metallization layer is also the first and second grid.

In response, Applicants direct the Examiner's attention to the preceding language within claim 1, wherein it is clearly described that the first and second grids are in respectively different design modules. The significance of this description is particularly clarified by the description in paragraph [0032], wherein it is described that the customary design procedure for integrated circuits is to have different engineering teams design different portions of the circuit, each corresponding to the claim terminology "different design module."

The significance of the terminology "first grid" and "second grid" is particularly clarified in the description in paragraphs [0034] and [0035], wherein it is further described that a "grid" is the point of the design module at which a relatively large number of components interconnect, such as a power grid or a ground for that design module. These grids can be (but are limited to) metallization layers within the design module, for example M1.

Therefore, the problem being addressed by the present invention is related to the common design practice of having different engineering teams separately developing distinct design modules within the integrated circuit.

In further response to the Examiner's confusion, the description in paragraph [0039] explains that the customary conventional design/fabrication process is that these grids for the separate design modules are not interconnected until final metallization, such as M5. The present inventors have observed that fabrication failures due to damage by overvoltages accumulating during plasma processing can be reduced by interconnecting these grids at an earlier fabrication stage, using one of various alternatives that may or may not be functional as part of the normal functioning of the circuit after it has been fabricated.

Relative to the Examiner's confusion concerning "said fabrication", it is brought to the

Examiner's attention that this terminology in the original claim referred back to the adjective use of "fabrication" in "a fabrication layer" and was, therefore, completely proper. However, in an effort to expedite prosecution, Applicants have amended the claim to preclude the possibility of an antecedent basis issue.

Relative to claim 4, wherein the Examiner alleges indefiniteness because "... a diffusion region is a source and a drain region" and the potential antecedent basis issue with "first metallization layer." Applicants have eliminated "first" from the claim to preclude this potential antecedent basis issue.

Relative to the Examiner's attempting to equate "diffusion region" with "source and drain regions", Applicants submit that, although the source and drain regions of a MOS device does include a diffusion region, not all diffusion regions serve the purpose of source and drain regions. That is, contrary to the Examiner's implication, there are many other purposes for which a diffusion region is used, including, for example, creating a well areas in a substrate, forming diodes, and establishing low resistance contact points. None of these alternative uses of a diffusion region provide a source or drain region. Therefore, Applicants submit that the Examiner's characterization that a "diffusion region" is equivalent to "source and drain regions" is incorrect.

Relative to claim 5, wherein the Examiner alleges indefiniteness because of the terminology "... an interconnect ... is conductive." Although Applicants cannot decipher the intended meaning of this rejection, it is submitted that the confusion seems to lie in the attempt to take selected wording out-of-the-context of that wording. That is, contrary to the characterization by the Examiner, the claim wording actually reads: "... an interconnect between said first grid and said second grid is conductive during said plasma processing and is non-conductive during an operation of said chip unless activated by a signal."

Applicants respectfully submit that, to one having ordinary skill in the art, this claim language is completely understood and no claim amendments are necessary to address this alleged indefiniteness issue, since this claim describes those embodiments in which the interconnect structure is active as a conductor only during the plasma processing but otherwise non-conductive. These concepts are discussed, for example, in paragraphs [0051] and [0054].

Relative to claim 6, wherein the Examiner alleges that the present invention fails to teach

this aspect of: "... wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip", Applicants direct the Examiner's attention to paragraph [0009], wherein it is described that conventional wisdom describes the SOI devices as isolated from the substrate.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTIONS

The examiner alleges that Liu anticipates claims 1-6, 8-10, and 19, and, when modified by Kimura, renders obvious claims 7 and 20.

Applicants respectfully disagree, since the present invention teaches that a different problem is causing the problem, thereby the environment of these two references fails to satisfy the plain meaning of the claim language of the independent claim.

More specifically, as explained in paragraph [0037], the present invention teaches that the damage to the chip components is due to two-dimensional differences in charging during the plasma process, so that, as shown in figure 2, different surfaces of the chip will receive different amount of charges. Therefore, the present invention teaches that, to overcome the damage done by this unequal distribution of charges, the different grids of different design modules should be interconnected before the first plasma operation after the grid has been formed. If these grids are not interconnected, as explained above, the plasma process will provide a different distribution of charges on the different grids, thereby causing a differential voltage between the grids.

Neither Liu nor Kimura suggests that the damage during the plasma process occurs as a result of a two-dimensional difference in distribution of charging. Therefore, neither reference refers to different design modules for which interconnection is necessary in order to prevent damage due to the plasma process over the two-dimensional surface.

The examiner attempts to define that labels 12 and 14 are two different design modules in Liu. However, Applicants submit that there is no indication in this reference that these two areas of the chip are two distinct design modules having two distinct grids. The Examiner has made this assumption without pointing to any lines in the reference for support. Therefore, until the Examiner provides a reasonable basis for this assertion, Applicants submit that the rejection

currently of record fails to meet the initial burden of a *prima facie* rejection, since the element has not been clearly identified in the reference. If the Examiner wishes to maintain this reduction on Liu, it is requested that a proper line and column in Liu be indicated on the record prior to proceeding to Appeal.

Moreover, contrary to the implication in the rejection, the plain language of the claim is not satisfied by primary reference Liu because the connection discussed for protection for plasma processing is to the substrate, not between the grids of two design modules. The reason is that the substrate is involved in the primary reference is that Liu is not based on SOI technology, as secondary reference Kimura and the present invention.

Hence, turning to the clear language of the claims, in Liu there is no teaching or suggestion of: "... wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process."

Relative to the Examiner's statement that the final claim limitation of the independent claims fails to have patentable weight, Applicants respectfully disagree, since one of ordinary skill in the art would consider that this description is structural in nature. That is, one of ordinary skill in the art would be able to discern from a cross-section of a chip, in conjunction with a knowledge of how chip fabrication occurs, whether the chip being evaluated has the structural features described in this final claim limitation wherein it is described that the two design modules are interconnected in a manner that precludes differential voltage accumulation during a plasma processing step. Applicants submit, therefore, that this entire claim limitation does indeed have patentable weight.

Relative to the rejection for claim 5, Applicants request that the Examiner identify specific column and line locations in Liu upon which the Examiner relies.

Relative to the rejection for claim 6, Applicants submit that Liu uses standard chip fabrication wherein the components are fabricated directly on the substrate and, therefore, inherently fails to satisfy the plain meaning of the claim language.

Relative to the rejection for claim 8, Applicants submit that the accumulation of charges, as the Examiner characterizes in the rejection, inherently indicates that the carriers are not migrating.

Finally, relative to the combination of secondary reference Kimura with Liu, Applicants submit that, because Kimura is based on SOI technology but Liu is not, these two references are non-analogous and cannot be combined.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Liu or Kimura, and the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-10, 19, and 20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

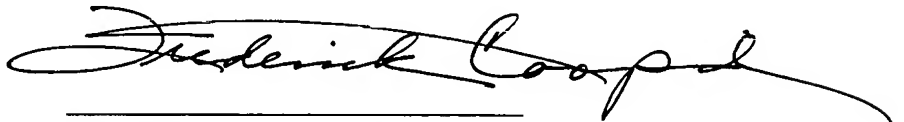
Moreover, Applicants submit that claims 11-18 are subject to rejoinder and, therefore, also allowable, and Applicants request such rejoinder of claims.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

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